



# **Advances in Analog and RF IC Design for Wireless Communication Systems: Chapter 12. Time-to-Digital Conversion for Digital Frequency Synthesizers**

*Michael H. Perrott*

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Time-to-digital converter (TDC) circuits are a key component for achieving high-performance digital phase-locked loops (PLLs) which offer lower area and greater flexibility than their analog PLL counterparts. This chapter focuses on a recently developed TDC architecture known as the gated ring oscillator (GRO) which offers first-order shaping of its quantization noise and delay stage mismatch. To provide context for the GRO discussion, background on general TDC implementation techniques is described along with key performance issues related to digital frequency synthesizers. The GRO concept is then presented, followed by implementation details and measured results. Finally, recent variations on the GRO concept are described such as a MASH TDC structure which achieves higher-order noise shaping and a switched ring oscillator (SRO) TDC which improves robustness to dead zones encountered by the GRO TDC.

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